

# **H1602B**

# **LCD MODULE MANUAL**

## **Character 16X2**

### **Contents**

1. Precautions in use of LCD Modules
2. General Specification
3. Absolute Maximum Ratings
4. Electrical Characteristics
5. Optical Characteristics
6. Interface Pin Function
7. Contour Drawing & Block Diagram
8. Function Description
9. Character Generator ROM Pattern
10. Instruction Table
11. Timing Characteristics
12. Backlight Information
13. Initializing of LCM

# **1. Precautions in use of LCD Modules**

- (1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
- (3) Don't disassemble the LCM.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist LCM.
- (6) Soldering: only to the I/O terminals.
- (7) Storage: please storage in anti-static electricity container and clean environment.

# **2. General Specification**

Item	Dimension	Unit
Number of Characters	16 characters x 2 Lines	-
Module dimension	80.0 x 36.0 x 13.2(MAX)	mm
View area	66.0 x 16.0	mm
Active area	56.2 x 11.5	mm
Dot size	0.55 x 0.65	mm
Dot pitch	0.60 x 0.70	mm
Character size	2.95 x 5.55	mm
Character pitch	3.55 x 5.95	mm
LCD type	STN, Positive	
Duty	1/16	
View direction	6 o'clock	
Backlight Type	LED	

# **3. Absolute Maximum Ratings**

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	$T_{OP}$	0	-	+50	-
Storage Temperature	$T_{ST}$	-10	-	+60	-
Input Voltage	$V_I$	$V_{SS}$	-	$V_{DD}$	V
Supply Voltage For Logic	$V_{DD}-V_{SS}$	-0.3	-	7	V
Supply Voltage For LCD	$V_{DD}-V_0$	-0.3	-	13	V

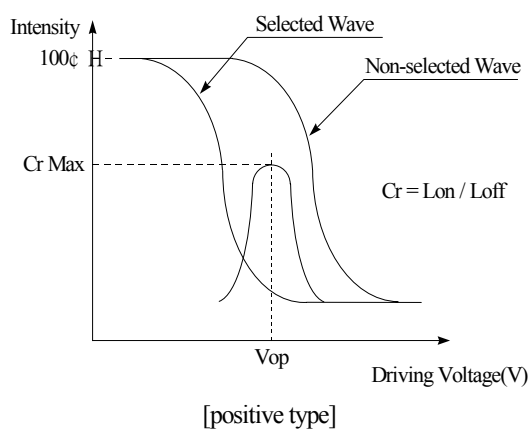
## 4. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	$V_{DD}-V_{SS}$	-	2.7	-	5.5	V
Supply Voltage For LCD	$V_{DD}-V_0$	$T_a=0^{\circ}\text{C}$	-	-	4.2	V
		$T_a=25^{\circ}\text{C}$	-	3.8	-	V
		$T_a=+50^{\circ}\text{C}$	3.4	-	-	V
Input High Volt.	$V_{IH}$	-	2.2	-	$V_{DD}$	V
Input Low Volt.	$V_{IL}$	-	-	-	0.6	V
Output High Volt.	$V_{OH}$	-	2.4	-	-	V
Output Low Volt.	$V_{OL}$	-	-	-	0.4	V
Supply Current	$I_{DD}$	$V_{DD}=5\text{V}$	-	1.2	-	mA

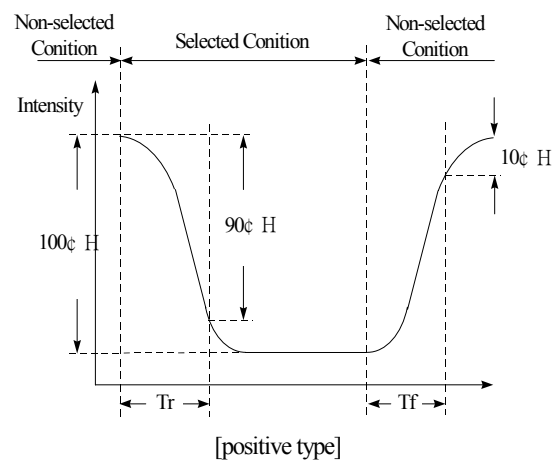
## 5. Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	$(V)\theta$	$CR \geq 2$	10	-	40	deg
	$(H)\phi$	$CR \geq 2$	-30	-	30	deg
Contrast Ratio	CR	-	-	3	-	-
Response Time	T rise	-	-	200	300	ms
	T fall	-	-	200	300	ms

### Definition of Operation Voltage ( $V_{op}$ )



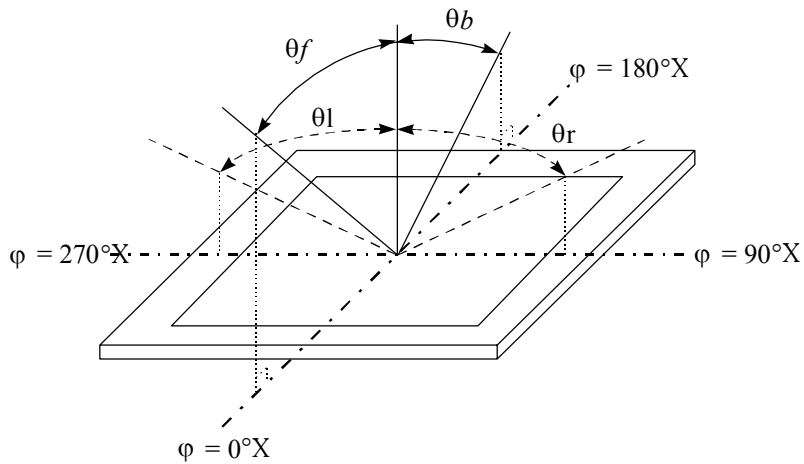
### Definition of Response Time ( $T_r$ , $T_f$ )



### Conditions :

Operating Voltage :  $V_{op}$       Viewing Angle( $\theta$ ) :  $0^{\circ}$   
 Frame Frequency : 64 HZ      Driving Waveform : 1/N duty , 1/a bias

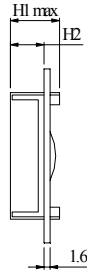
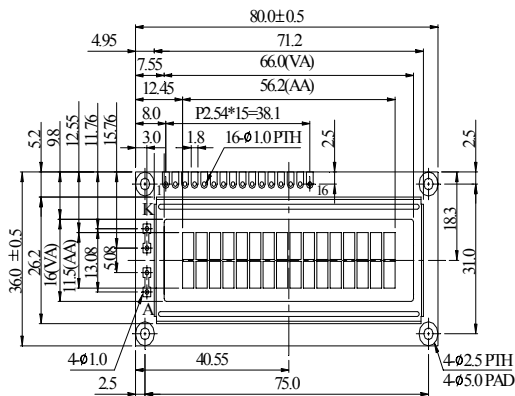
## Definition of viewing angle(CR≥2)



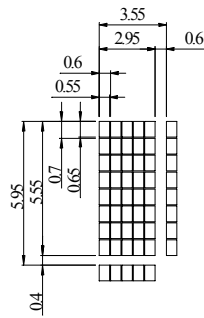
## 6. Interface Pin Function

Pin No.	Symbol	Level	Description
1	V <sub>SS</sub>	0V	Ground
2	V <sub>DD</sub>	5.0V	Supply Voltage for logic
3	VO	(Variable)	Operating voltage for LCD
4	RS	H/L	H: DATA, L: Instruction code
5	R/W	H/L	H: Read(MPU←Module) L: Write(MPU→Module)
6	E	H,H→L	Chip enable signal
7	DB0	H/L	Data bit 0
8	DB1	H/L	Data bit 1
9	DB2	H/L	Data bit 2
10	DB3	H/L	Data bit 3
11	DB4	H/L	Data bit 4
12	DB5	H/L	Data bit 5
13	DB6	H/L	Data bit 6
14	DB7	H/L	Data bit 7
15	A	4.2V-4.6V	LED +
16	K	0V	LED -

# 7. Contour Drawing & Block Diagram



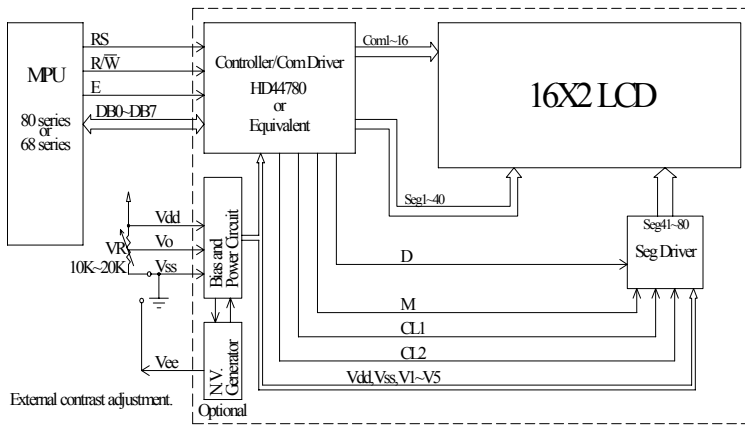
LEDBL	
H1	13.2
H2	8.6



DOT SIZE

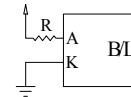
The non-specified tolerance of dimension is  $\pm 0.3\text{mm}$

PIN NO.	SYMBOL
1	Vss
2	Vdd
3	Vo
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	A/Vee
16	K

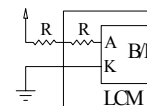


### LEDBL Drive Method

1. Drive from AK



2. Drive from pin15, pin16



(Will never get Vee output from pin15)

Character located	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
DDRAM address	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

## 8. Function Description

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB7)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

### Busy Flag (BF)

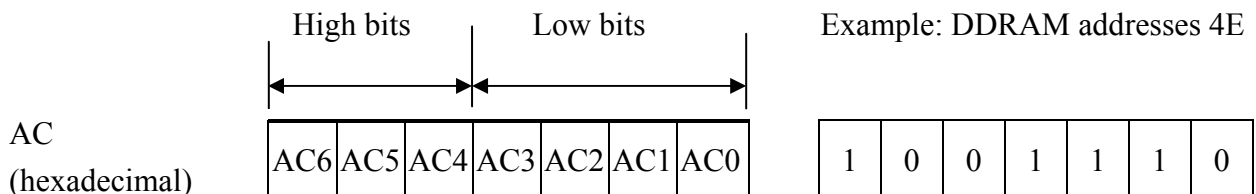
When the busy flag is 1, the controller LSI is in the internal operation mode, and the next instruction will not be accepted. When RS=0 and R/W=1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

### Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM

### Display Data RAM (DDRAM)

This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80×8 bits or 80 characters. Below figure is the relationships between DDRAM addresses and positions on the liquid crystal display.



Display position DDRAM address

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

2-Line by 16-Character Display

**Character Generator ROM (CGROM)**

The CGROM generate 5×8 dot or 5×10 dot character patterns from 8-bit character codes. See Table 2.

**Character Generator RAM (CGRAM)**

In CGRAM, the user can rewrite character by program. For 5×8 dots, eight character patterns can be written, and for 5×10 dots, four character patterns can be written.

Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.

# Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns

**Table 1.**

For 5 \* 8 dot character patterns

Character Codes ( DDRAM data )		CGRAM Address		Character Patterns ( CGRAM data )			
7 6 5 4 3 2 1 0		5 4 3 2 1 0		7 6 5 4 3 2 1 0			
High Low		High Low		High Low			
0 0 0 0 * 0 0 0		0 0 0	0 0 0	* * *		Character pattern( 1 )	
			0 0 1	* * *			0 0 0
			0 1 0	* * *			0 0 0
			0 1 1	* * *			0
			1 0 0	* * *			0 0 0 0
			1 0 1	* * *			0 0 0 0
			1 1 0	* * *			0 0 0 0
			1 1 1	* * *			0 0 0 0
			0 0 0	* * *			0 0 0 0
			0 0 1	* * *			0 0 0 0
0 0 0 0 * 0 0 1		0 0 1	1 0 0	* * *		Character pattern( 2 )	
			1 0 1	* * *			0 0 0 0
			1 1 0	* * *			0 0 0 0
			1 1 1	* * *			0 0 0 0
			0 0 0	* * *			0 0 0 0
			0 0 1	* * *			0 0 0 0
			0 1 0	* * *			0 0 0 0
			0 1 1	* * *			0 0 0 0
			1 0 0	* * *			0 0 0 0
			1 0 1	* * *			0 0 0 0
			0 0 0	* * *			
			0 0 1	* * *			

For 5 \* 10 dot character patterns

Character Codes ( DDRAM data )		CGRAM Address		Character Patterns ( CGRAM data )			
7 6 5 4 3 2 1 0		5 4 3 2 1 0		7 6 5 4 3 2 1 0			
High Low		High Low		High Low			
0 0 0 0 * 0 0 0		0 0	0 0 0 0	* * *		Character pattern	
			0 0 0 1	* * *			0 0 0 0 0
			0 0 1 0	* * *			0 0 0 0 0
			0 0 1 1	* * *			0 0 0 0
			0 1 0 0	* * *			0 0 0 0
			0 1 0 1	* * *			0 0 0 0
			0 1 1 0	* * *			0 0 0 0
			0 1 1 1	* * *			0 0 0 0
			1 0 0 0	* * *			0 0 0 0
			1 0 0 1	* * *			0 0 0 0
			1 0 1 0	* * *	0 0 0 0 0	Cursor pattern	
			1 1 1 1	* * *	* * * * *		

■ : " High "

# 9. Character Generator ROM Pattern

Table.2

Upper 4 bit Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)			0	1	2	3	4				5	6	7	8	9
LLLH	(2)		!	0	1	2	3	4			5	6	7	8	9	:
LLHL	(3)		"	0	1	2	3	4			5	6	7	8	9	;
LLHH	(4)		#	0	1	2	3	4			5	6	7	8	9	<
LHLL	(5)		\$	0	1	2	3	4			5	6	7	8	9	=
LHLH	(6)		%	0	1	2	3	4			5	6	7	8	9	>
LHHL	(7)		&	0	1	2	3	4			5	6	7	8	9	?
LHHH	(8)		'	0	1	2	3	4			5	6	7	8	9	@
HLLL	(1)		(	0	1	2	3	4			5	6	7	8	9	^
HLLH	(2)		)	0	1	2	3	4			5	6	7	8	9	_
HLHL	(3)		*	0	1	2	3	4			5	6	7	8	9	~
HLHH	(4)		+	0	1	2	3	4			5	6	7	8	9	~
HHLL	(5)		,	0	1	2	3	4			5	6	7	8	9	~
HHLH	(6)		-	0	1	2	3	4			5	6	7	8	9	~
HHHL	(7)		.	0	1	2	3	4			5	6	7	8	9	~
HHHH	(8)		/	0	1	2	3	4			5	6	7	8	9	~

# 10. Instruction Table

Instruction	Instruction Code										Description	Execution time (fosc=270Khz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "00H" to DDRAM and set DDRAM address to "00H" from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	*	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and enable the shift of entire display.	39μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.	39μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Set interface data length (DL:8-bit/4-bit), numbers of display line (N:2-line/1-line)and, display font type (F:5×11 dots/5×8 dots)	39μs
Set CGRAM Address	0	0	0	1	ACG						Set CGRAM address in address counter.	39μs
Set DDRAM Address	0	0	1	ADD						Set DDRAM address in address counter.	39μs	
Read Busy Flag and Address	0	1	BF	AC						Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0μs	
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43μs

I/D = 1 : Increment

C = 1 : Cursor ON

R/L = 1 : Right Shift

F = 0 : 5x8 Dots

I/D = 0 : Decrement

C = 0 : Cursor OFF

R/L = 0 : Left Shift

F = 1 : 5x11 Dots

S = 1 : Display shift

B = 1 : Blink ON

DL = 1 : 8 Bits

BF = 1 : Busy

S = 0 : No display shift

B = 0 : Blink OFF

DL = 0 : 4 Bits

BF = 0 : Can Accept Data

D = 1 : Display ON

S/C = 1 : Display Shift

N = 1 : 2 Lines

A<sub>CG</sub> : CG RAM Address

D = 0 : Display OFF

S/C = 0 : Cursor Move

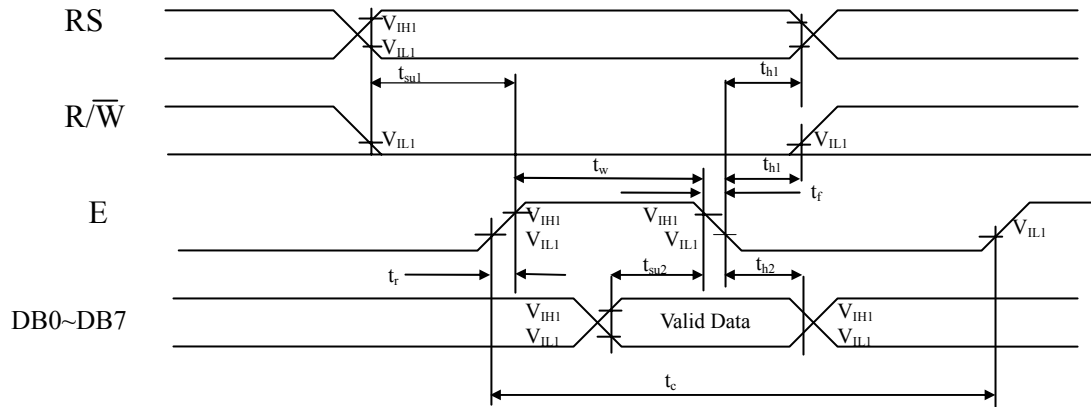
N = 0 : 1 Line

A<sub>DD</sub> : DD RAM Address

\* : don't care

# 11. Timing Characteristics

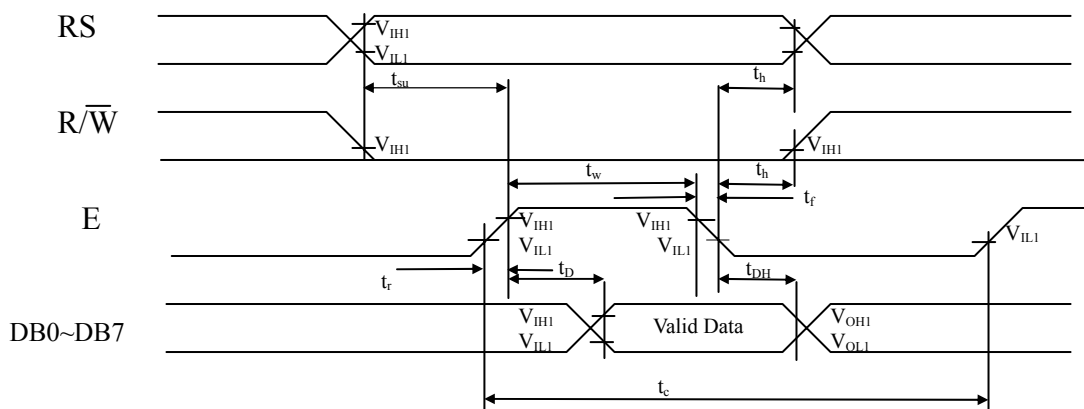
## 11.1 Write Operation



$V_{DD} = 4.5V \sim 5.5V$ ,  $T_a = -30^{\circ}C \sim 85^{\circ}C$

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode	E cycle Time	$t_c$	500	-	-	ns
	E Rise/Fall Time	$t_R, t_F$	-	-	20	
	E Pulse Width (High, Low)	$t_w$	230	-	-	
	R/W and RS Setup Time	$t_{su1}$	40	-	-	
	R/W and RS Hold Time	$t_{h1}$	10	-	-	
	Data Setup Time	$t_{su2}$	80	-	-	
	Data Hold Time	$t_{h2}$	10	-	-	

## 11.2 Read Operation



$V_{DD} = 4.5V \sim 5.5V$  ,  $T_a = -30^{\circ}C \sim 85^{\circ}C$

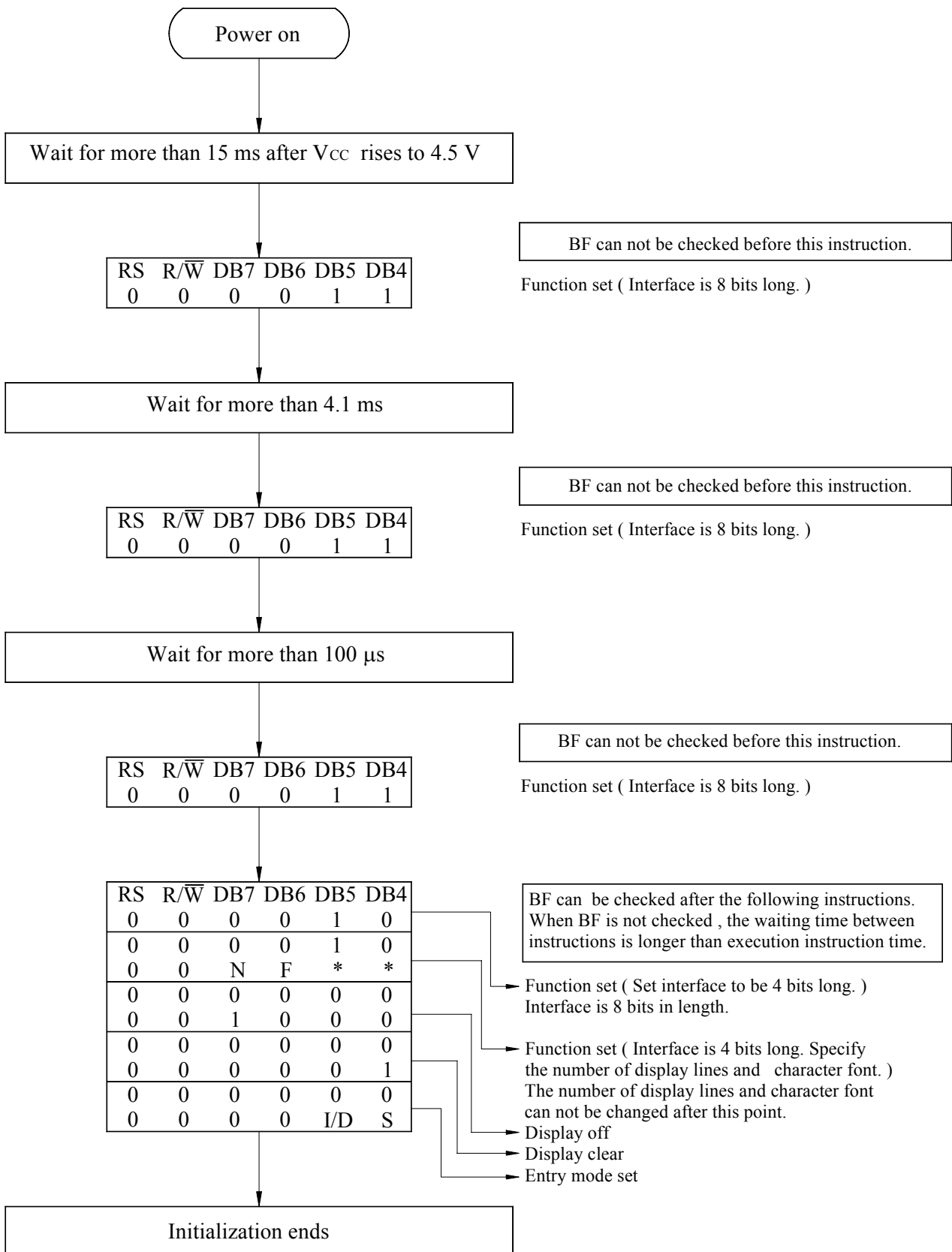
Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Read Mode	E cycle Time	$t_c$	500	-	-	ns
	E Rise/Fall Time	$t_R, t_F$	-	-	20	
	E Pulse Width (High, Low)	$t_w$	230	-	-	
	R/W and RS Setup Time	$t_{su}$	40	-	-	
	R/W and RS Hold Time	$t_H$	10	-	-	
	Data Output Delay Time	$t_D$	-	-	120	
	Data Hold Time	$t_{DH}$	5	-	-	

## **12. Backlight Information**

### **Specification**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST-CONDITION
Supply Current	I <sub>LED</sub>	-	130	260	mA	V=4.2V
Supply Voltage	V	-	4.2	4.6	V	-
Reverse Voltage	V <sub>R</sub>	-	-	8	V	-
Luminous Intensity	I <sub>V</sub>	-	85	-	CD/M <sup>2</sup>	I <sub>LED</sub> =130mA
Wave Length	$\lambda_p$	-	574	-	nm	I <sub>LED</sub> =130mA





4-Bit Interface